REMARKS

Applicants respectfully request consideration of this application. The following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

Claims 1, 5 – 7, 8 – 12, and 13 – 16 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,223,445 to Fuse ("Fuse"). Claims 2 – 4 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Fuse in view of U.S. Patent No. 6,248,652 to Kokubun ("Kokubun"). Claim 14 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Fuse and further in view of U.S. Patent No. 6,288,425 of Adan ("Adan").

35 U.S.C. § 102(b) Rejections

Independent claim 1 provides:

> A transistor device, comprising:
>
> a substrate having a source region, a drain region and a channel region, in which at least one of the source, drain and channel regions has **a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress**; and
>
> a gate region formed over the channel region. (emphasis added)

Fuse discloses a large angle ion implantation method being capable of forming amorphous layers in a semiconductor substrate. Ion implantation is accomplished using a rotating or stepping rotating implanting method wherein the implantation angle of an arsenic ion beam 4 is varied from 20 to 60 degrees. Under these implanting conditions an n-type layer 5 is formed in a proper depth of the

substrate 1 and an amorphous layer 6 is formed on the n-type layer 5. These two layers 5 and 6 were formed buried beneath the side wall 3. (Fuse, col. 4, lines 6 – 10, and FIG. 1(a)). Fuse also discloses:

> [T]he angle of the bottom corner of the amorphous layer 6 becomes dull. This means that two directions of crystal regrowth indicated by reference numerals 7 and 8 which is caused by a later heat treatment never meet with each other in the amorphous layer 6. In other words, crystal regrowth starting from the bottom and the side at the corner thereof never interfere with each other and, accordingly, **no large voids forming nuclei of defects are generated therein during the heat treatment**."
> (Fuse, col. 4, lines 11 – 22, and FIG. 1(b)).

Nothing in Fuse discloses a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress.

In contrast, independent claim 1 includes the limitation of "a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress." The Office Action states that Fuse teaches a transistor comprising source and drain regions having a void to place one of the regions into a comprehensive or tensile stress to alter carrier mobility due to the stress, directing Applicants to col. 1, lines 25 – 40, line 63 to line 13 of col. 2, and FIG. 14a. (Office Action dated 06/24/03, page 2, paragraph 5). Applicants respectfully submit that here, the Office Action is pointing Applicants to the Background of the Invention section in which Fuse discusses the problems in the prior art; in particular, substrate defects that occur as a result of voids formed during crystal regrowth. Moreover, there is no disclosure in Fuse (including the Background of the Invention) of voids to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the

stress. In fact, the method disclosed by Fuse is to **prev nt** the formation of voids in the substrate.

Therefore, Applicants respectfully submit that claim 1 is not anticipated by Fuse under 35 U.S.C. § 102(b) and respectfully request the withdrawal of the rejection of the claim. Claims 6 and 7 depend directly from independent claim 1, and thus include the limitation of "a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress." As such, Applicants respectfully submit that claims 6 and 7 are also not anticipated by Fuse under 35 U.S.C. § 102(b) and respectfully request the withdrawal of the rejection of the claims.

Independent claim 8 provides:

A transistor, comprising:

a substrate having a source region, a drain region and a channel region, in which **a void is located below the source region to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress**; and

a gate region above the channel region. (emphasis added)

Fuse discloses a large angle ion implantation method being capable of forming amorphous layers in a semiconductor substrate. Ion implantation is accomplished using a rotating or stepping rotating implanting method wherein the implantation angle of an arsenic ion beam 4 is varied from 20 to 60 degrees. Under these implanting conditions an n-type layer 5 is formed in a proper depth of the substrate 1 and an amorphous layer 6 is formed on the n-type layer 5. These two layers 5 and 6 were formed buried beneath the side wall 3. (Fuse, col. 4, lines 6 –

10, and FIG. 1(a)). Fuse also discloses:

> [T]he angle of the bottom corner of the amorphous layer 6 becomes dull. This means that two directions of crystal regrowth indicated by reference numerals 7 and 8 which is caused by a later heat treatment never meet with each other in the amorphous layer 6. In other words, crystal regrowth starting from the bottom and the side at the corner thereof never interfere with each other and, accordingly, **no large voids forming nuclei of defects are generated therein during the heat treatment**."
> (Fuse, col. 4, lines 11 – 22, and FIG. 1(b)).

Nothing in Fuse discloses a void is located below the source region to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress.

In contrast, independent claim 8 includes the limitation, "a void is located below the source region to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress." The Office Action states that Fuse teaches a transistor in which a void is located below the source region to place one of the regions into a comprehensive or tensile stress to alter carrier mobility due to the stress, directing Applicants to col. 1, lines 25 – 40, line 63 to line 13 of col. 2, and FIG. 14a. (Office Action dated 06/24/03, page 4, paragraph 4). Applicants respectfully submit that here, the Office Action is directing Applicants to the Background of the Invention section in which Fuse discusses the problems in the prior art; in particular, substrate defects that occur as a result of voids formed during crystal regrowth. Moreover, there is no disclosure in Fuse (including the Background of the Invention) of a void located below the source region to place one of the regions into a compressive or tensile stress to alter

carrier mobility due to the stress. In fact, the method disclosed by Fuse is to **pr v nt** the formation of voids in the substrate.

Therefore, Applicants respectfully submit that claim 8 is not anticipated by Fuse under 35 U.S.C. § 102(b) and respectfully request the withdrawal of the rejection of the claim. Claims 9 – 14 either directly or indirectly depend from independent claim 8, and thus include the limitation, "a void is located below the source region to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress." As such, Applicants respectfully submit that claims 9 – 14 are also not anticipated by Fuse under 35 U.S.C. § 102(b) and respectfully request the withdrawal of the rejection of the claims.

Independent claim 15 provides:

A transistor comprising:

a substrate having a source region, a drain region and a channel region; and

a gate region having a void to place the substrate under mechanical stress to alter carrier mobility due to the stress. (emphasis added)

Fuse discloses a large angle ion implantation method being capable of forming amorphous layers in a semiconductor substrate. Ion implantation is accomplished using a rotating or stepping rotating implanting method wherein the implantation angle of an arsenic ion beam 4 is varied from 20 to 60 degrees. Under these implanting conditions an n-type layer 5 is formed in a proper depth of the substrate 1 and an amorphous layer 6 is formed on the n-type layer 5. These two layers 5 and 6 were formed buried beneath the side wall 3. (Fuse, col. 4, lines 6 –

10, and FIG. 1(a)). Fuse also discloses:

> [T]he angle of the bottom corner of the amorphous layer 6 becomes dull. This means that two directions of crystal regrowth indicated by reference numerals 7 and 8 which is caused by a later heat treatment never meet with each other in the amorphous layer 6. In other words, crystal regrowth starting from the bottom and the side at the corner thereof never interfere with each other and, accordingly, **no large voids forming nuclei of defects are generated therein during the heat treatment.**"
> (Fuse, col. 4, lines 11 – 22, and FIG. 1(b)).

Nothing in Fuse discloses a gate region having a void to place the substrate under mechanical stress to alter carrier mobility due to the stress.

In contrast, independent claim 15 includes the limitation of "a gate region having a void to place the substrate under mechanical stress to alter carrier mobility due to the stress." The Office Action states that Fuse teaches a transistor with a gate region having a void to place the substrate under mechanical stress to alter carrier mobility due to the stress, directing Applicants to col. 1, lines 25 – 40, line 63 to line 13 of col. 2, and FIG. 14a. (Office Action dated 06/24/03, page 4, paragraph 4). Applicants respectfully submit that here, the Office Action is directing Applicants to the Background of the Invention section in which Fuse discusses the problems in the prior art; in particular, substrate defects that occur as a result of voids formed during crystal regrowth. Moreover, there is no disclosure in Fuse (including the Background of the Invention) of a gate region having a void to place the substrate under mechanical stress to alter carrier mobility due to the stress. In fact, the method disclosed by Fuse is to **pr vent** the formation of voids in the substrate.

Therefore, Applicants respectfully submit that claim 15 is not anticipated by Fuse under 35 U.S.C. § 102(b) and respectfully request the withdrawal of the rejection of the claim. Claims 17 and 18 directly depend from independent claim 15, and thus include the limitation of "a gate region having a void to place the substrate under mechanical stress to alter carrier mobility due to the stress." As such, Applicants respectfully submit that claims 17 and 18 are also not anticipated by Fuse under 35 U.S.C. § 102(b) and respectfully request the withdrawal of the rejection of the claims.

35 U.S.C. § 103(a) Rejections

Claims 2 – 4 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Fuse in view of Kokubun. Claims 2 – 4 depend directly from independent claim 1 and thus include the limitation of "a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress."

As discussed above, Fuse does not teach or suggest a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress. Kokubun discloses a semiconductor device that suppresses short channel effects. An insulating layer 10 of preferably dielectric material (e.g. nitride layer) of about 50 nm thickness is formed on layer 9 by using a CVD method and a thicker insulating layer 7 of preferably dielectric material (e.g. silicon dioxide) of about 500 nm is formed over the layer 9 by a CVD method. By using a photolithography method, the layers 7 and 10 at predetermined locations are removed to form a groove 21. Then, using the thicker layer 7 as a mask, a dopant (e.g. Boron ion) is

introduced into the semiconductor substrate 1 by using an ion implantation method (accelerated energy 60 kev, dose quantity 8.times.10.sup.12 cm.sup.-2) and a heat treatment is performed to form a p-type of heavily doped region 11, which is the same type as the semiconductor substrate 1. (Kokubun, col. 4, lines 2 – 16, and FIGS. 1a and 1b). Nothing in Kokubun teaches or suggests a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress. The Office Action states that Kokubun discloses a void 4 located substantially in a center of the channel region, making reference to FIGS. 7A – 7C. (Office Action dated 6/24/03, page 3, paragraph 6). Applicants respectfully submit that FIGS. 7A – 7C in fact refer to prior art MOS transistors in which a p-type heavily doped region 4 is directly under gate electrodes 5. (Kokubun, col. 2, lines 1 – 2). As such, Kokubun fails to cure the deficiency of Fuse. Therefore, Applicants respectfully submit that claim 1 is not unpatentable over the combination of Fuse in view of Kokubun and request withdrawal of the rejection.

It is respectfully submitted that Fuse and Kokubun do not teach or suggest a combination with each other. Applicants respectfully submit that it would be impermissible hindsight, based on Applicants' own disclosure to combine Fuse and Kokubun.

Applicants also respectfully submit that there is no motivation to combine Fuse and Kokubun. The Office Action states, "It would have been obvious to one of ordinary skill in the art, at the time the invention was made to form the void which is located substantially in a center of the channel region, as taught by Kokubun in order to obtain suitable device for desired application." (Office Action dated 06/24/2003,

page 3, lines 16 – 17 and page 4, lines 1 – 2). Here, the Office Action merely states an advantage of substituting a step in the method from Kokubun with a step in Fuse without explaining what specific understanding or technological principle within the knowledge of one of ordinary skill in the art would have suggested the combination. In fact, as discussed above, Fuse teaches away from forming voids in the substrate.

Even if Fuse and Kokubun were combined, the combination would still not result in the limitations of claim 1. In particular, Fuse and Kokubun do not include the limitation "a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress." The heavily doped region formed in the substrate of Kokubun is clearly not a void. As Fuse and Kokubun, alone or in combination, do not teach all the limitations of claim 1, the combination cannot be interpreted do disclose the limitations of claim 1. Therefore, Applicants respectfully request the withdrawal of the rejection of dependent claims 2 – 4 under 35 U.S.C. § 103(a) over the combination.

Claim 14 has been rejected under 35 U.S.C. §103(a) as being unpatentable over Fuse and further in view of Adan. Claim 14 depends directly from independent claim 8 and thus includes the limitation of "a void is located below the source region to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress."

As discussed above, Fuse does not teach or suggest a void located below the source region to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress. Adan discloses a SOI.MOSFET having an embedded region of a second conductivity type disposed between the source/drain

regions in the top semiconductor layer and underneath the gate electrode and separated from the source/drain regions and from a top semiconductor/gate oxide interface. (Adan, col. 4, lines 37 – 42). Adan also discloses that the embedded region 6 is N-type which is the same conductivity type as the source/drain regions 13 and which is different from the conductivity type of the surface channel. The embedded region 6 is separated from the source/drain regions 13 and from the gate oxide/surface channel interface. Although the embedded region 6 is floating, the embedded region 6 is in contact with the buried oxide 2 and is capacitively coupled to the substrate potential through a capacitor formed by the embedded region 6, the buried oxide film 2 and the substrate 1. (Adan, col. 7, lines 18 – 27, and FIG. 1). Nothing in Adan teaches or suggests a void located below the source region to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress. As such, Adan fails to cure the deficiency of Fuse. Therefore, Applicants respectfully submit that claim 8 is not unpatentable over the combination of Fuse in view of Adan and request withdrawal of the rejection.

It is respectfully submitted that Fuse and Adan do not teach or suggest a combination with each other. Applicants respectfully submit that it would be impermissible hindsight, based on Applicants' own disclosure to combine Fuse and Adan.

Applicants also respectfully submit that there is no motivation to combine Fuse and Adan. The Office Action states, "It would have been obvious to one of ordinary skill in the art, at the time the invention was made to form the gate region of metal as taught by Adan in Fuse's device because the material such as polysilicon

and metal are recognized equivalent materials for forming the gate region of a transistor and they are interchangeable." (Office Action dated 06/24/2003, page 5, lines 10 – 14). Here, the Office Action merely states an advantage of substituting a material from Adan with a material from Fuse without explaining what specific understanding or technological principle within the knowledge of one of ordinary skill in the art would have suggested the combination.

Even if Fuse and Adan were combined, the combination would still not result in the limitations of claim 1. In particular, Fuse and Adan do not include the limitation "a void to place one of the regions into a compressive or tensile stress to alter carrier mobility due to the stress." As Fuse and Adan, alone or in combination, do not teach all the limitations of claim 8, the combination cannot be interpreted do disclose the limitations of claim 8. Therefore, Applicants respectfully request the withdrawal of the rejection of dependent claim 14 under 35 U.S.C. § 103(a) over the combination.

The Office Action Summary states that a shortened statutory period for reply is set to expire 2 months from the mailing date of the Office Action (06/24/03). However, the body of the Office Action states that the period for reply is set to expire 3 months from the mailing date (page 6, paragraph 6). Examiner Le confirmed the 3-month reply period during a teleconference with Suk Lee on July 15, 2003.

If the allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Suk Lee at (408) 720-8300. If there are any additional charges, please charge our Deposit Account No. 02–2666.

Respectfully submitted,

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